## AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

Claims 1-31. (Canceled)

32. (Currently Amended) An integrated circuit comprising:

a reflective layer having a reflective upper surface defining a first interface;

a first anti-reflective coating layer formed over the reflective layer, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a second interface;

a second anti-reflective coating layer formed over said first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a third interface, wherein the first, second, and third interface reflects radiation, and wherein the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coating layers are such that the amplitudes are approximately equal and the phase differences of the reflected radiation from said first, second, and third interfaces substantially mutually cancel when combined;

a dielectric layer formed on said second anti-reflective coating layer; [[and]]

an opening formed in said dielectric layer to expose said second anti-reflective coating layer; and

a metal layer formed over said dielectric layer and into said opening.

Claims 33-35 (Canceled).

36. (Previously presented) The integrated circuit according to claim 32, further comprising at least one additional anti-reflective coating layer formed between the second anti-reflective coating layer and the dielectric layer.

37. (Canceled).

38. (Previously presented) The integrated circuit according to claim 32, wherein the thickness of the first anti-reflective coating layer is approximately from 10 to 60 nanometers and the thickness of the second anti-reflective coating layer is approximately from 10 to 40 nanometers.

39. (Original) The integrated circuit according to claim 32, wherein the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

40. (Currently Amended) A memory cell comprising:

a structure on a substrate, the structure comprising:

at least two active areas formed in the substrate;

a gate stack between the active areas;

a capacitor electrically coupled with one of the active areas;

a first anti-reflective coating layer formed over the structure, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface;

a second anti-reflective coating layer formed on at least a portion of the first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface;

an insulating layer formed on the second anti-reflective coating layer; [[and]]

an opening formed in said insulating layer to expose said second anti-reflective coating layer; and

a metal layer formed over said insulating layer and into said opening.

41. (Canceled).

42. (Previously presented) The memory cell according to claim 40, wherein the second anti-reflective coating layer is formed on said first anti-reflective coating layer.

43. (Canceled).

44. (Previously presented) The memory cell according to claim 40, wherein the structure is a dual DRAM cell structure comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical communication with the first active area, the second capacitor being in electrical communication with the third active area, and the second active area being in electrical communication with a bit line.

45. (Original) The memory cell according to claim 44, wherein the capacitors are formed over the gate stacks.

46. (Original) The memory cell according to claim 45, wherein the capacitors are container capacitors.

47. (Original) The memory cell according to claim 44, wherein the bit line is formed over the capacitors.

48. (Previously presented) The memory cell according to claim 40, wherein the thickness of the first anti-reflective coating layer is approximately from 10 to 60 nanometers and the thickness of the second anti-reflective coating layer is approximately from 10 to 40 nanometers.

49. (Canceled).

50. (Currently Amended) An integrated circuit comprising:

at least one memory cell, the memory cell comprising:

a structure on a substrate, the structure comprising:

at least two active areas formed in the substrate;

a gate stack between the active areas;

a capacitor in electrical contact with one of the active areas;

an etch stop layer comprising:

a first anti-reflective coating layer formed over the structure;

a second anti-reflective coating layer formed over at least a portion of the first anti-reflective coating layer;

an insulating layer formed on the etch stop layer; [[and]]

an opening formed in said insulating layer to expose said second anti-reflective coating layer; and

a metal layer formed over said insulating layer and into said opening.

Claims 51-63 (Canceled).